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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/975,364

10/11/2001

Edwin Park

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9521

23494

7590

12/07/2006

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EXAMINER

CHEN, ALAN S

ART UNIT

PAPER NUMBER

2182

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/975,364	PARK, EDWIN	
	<b>Examiner</b>	<b>Art Unit</b>	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 22 November 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-6,8 and 9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-6,8 and 9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. In view of the Appeal Brief filed on 10/04/2006, PROSECUTION IS HEREBY REOPENED. A new ground of rejection based on 35 U.S.C. §112 first and second paragraphs is set forth below. The rejection has been made to better clarify the claims and the prosecution record as to the metes and bounds of the claims.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid. A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below at the end of this Office Action.

### ***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1,2,4-6,8 and 9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter

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which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically in Claim 1, the Applicant claims, "...a universal interface device **concurrently** interfaces with the plurality of different peripheral devices using **time multiplexing**...". "Time multiplexing" is defined as each peripheral device being allocated separate time slots for communications, time-multiplexing *cannot* be 'concurrent' since the peripheral devices are not operating simultaneously in time. The specification does not disclose how the time slots are allocated and conflicts with the claim language given that time multiplexing, by definition, cannot be concurrent. Claims 2,4-6,8 and 9 are rejected based on being dependent on rejected claim 1.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1,2,4-6,8 and 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is the indefinite as to the meaning of "time multiplexing" in claim 1, where the word "concurrently" in claim 1, implies time multiplexing is simultaneous, while time multiplexing, requires switching between multiple time slots and is not simultaneous. Examiner will assume "time multiplexing" as used in the claims do not require time slots and switching therein. Examiner recommends applicant use the lexicon "time-division multiplexing" instead of "time multiplexing" since it is more common and well-known to

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one of ordinary skill in the art. Claims 2,4-6,8 and 9 are rejected as being dependent on a rejected claim 1.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1 and 5 rejected under 35 USC 103(a) as being unpatentable over US Pat. 6,973,658 to Nguyen in view of US Pat. No. 4,041,473 to Bardotti et al. (*Bardotti*).

9. Per claim 1, Nguyen discloses a universal interface device (*Fig. 1, element 100*), comprising: a controller (*Fig. 1, element 105*); a configuration database coupled to the controller (*Fig. 2, element 210 and Fig. 1, MEMORY element connected to controller; Column 7, lines 50+, discloses storing various drivers, programs, etc, which by definition, is a configuration database*), said configuration database having stored therein a plurality of different configuration protocols (*Column 7, lines 50+, expressly states memory, element 210, "...is used primarily for storing...initialization program,*

*main program...connector cores, device driver,...", connector cores clearly being protocols for the different connections, see Column 4, lines 48-59) for supporting a plurality of different peripheral devices (Fig. 1, elements 184-194 are the various devices working over different protocols); a plurality of interconnection pads (Fig. 1, elements 124-129 are the ports/pads/pins associated with each peripheral device); a memory (Fig. 2, element 272, internal memory to the programmable unit in Fig. 1; Column 8, lines 5-10 disclose the memory being RAM) coupled to the interconnection pads and controller, the memory is programmable by the controller in order to support any of the different peripheral devices (Fig. 2, shows internal memory used to support various protocols); and a multiplexer coupled between the memory and the plurality of interconnection pads (Column 13, lines 58-60, the multiplexer is inside the programmable unit, Fig. 1, element 115) wherein the universal interface device concurrently interfaces with the plurality of different peripheral devices using time multiplexing of the plurality of interconnections pads (Column 9, lines 3+ disclose "periodically" polling the various I/O ports, elements 125-129 for connection of a external device; this suffices to meet the "time multiplexing" since polling is done with respect to time; Column 6, lines 30+ further discloses having switching matrix; Column 4, lines 25-31 explicitly states two or more peripheral devices connected in communicating).*

Nguyen does not disclose expressly time multiplexing being in the form of time division multiplexing where each peripheral device is given a fixed time slot.

Bardotti discloses what has been common practice for those of ordinary skill in the art, where a plurality of peripheral devices (*Fig. 1, elements 4 and 5*) are allocated a fixed time slot over a single physical channel such that each peripheral communicates over the channel at fixed intervals in time (*Column 3, lines 43-49*).

Nguyen and Bardotti are analogous art because they are from the same field of endeavor in communicating with multiple peripheral devices connected to a single controller having limited physical communication channels to a host.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use time division multiplexing. The suggestion/motivation for doing so would have been to utilize an effective and generations old technique that enables multiple devices to communicate over a share physical communication line.

10. Per claim 5, Nguyen combined with Bardotti discloses claim 1, Nguyen further disclosing the controller selecting the configuration protocol amongst the plurality of protocols (*Column 5, lines 43-55*) in the configuration database (*Column 5, lines 43-55, connector cores stored in configuration database storage, element 120 executed by controller*) to configure the memory and support the active peripheral device (*Fig. 2, element 272 configured to support active peripheral*).

11. Claims 2,4,6,8 and 9 are rejected under 35 USC 103(a) as being unpatentable over Nguyen in view of Bardotti in further view of US Pat. 6,742,071 to Boynton et al. (*Boynton*).

Nguyen combined with Bardotti discloses claim 1.

Nguyen combined with Bardotti does not disclose expressly the use a state machine in the controller and what is required of a state machine that controls a universal interface device. Nguyen combined with Bardotti also does not disclose a programmable clock coupled to the memory.

Boynton discloses a universal interface device capable of interface various external inputs (*Fig. 4; Column 2, lines 30+*). Boynton expressly discloses the need for a state machine to handle various situations presented by a universal interface device, where the input signals vary depending on the protocol (*Fig. 13 and 14, different read/write and control signals determine how the interface device needs to operate, the operation determined by the state machine*). Boynton further discloses the state logic (*Fig. 13 and 14*) interoperating with various parts other digital hardware, as well as the state logic interacting with tri-state devices (*Fig. 13 and 14, element 163*). Boynton also discloses the need for a programmable clock signal (*Column 2, lines 35-40*).

Nguyen combined with Bardotti and Boynton are analogous art because they are from similar problem solving area in interfacing multiple devices each operating with a different communication protocol, many of the protocols being the same, e.g., USB, and other asynchronous, isochronous, synchronous protocols.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a state machine in Nguyen combined with Bardotti with the associated logic necessary to communicate with multiple different protocol devices and having a programmable clock signal.



The suggestion/motivation for doing so would have been it being well-known in digital design that state machines operate to oversee and guide how the overall digital logic operate, and in particular, for state machines used in universal interface devices, programmable routing, mapping, programmable clocks, etc. are needed in order to interface with various communication protocols that operate at different frequencies, and require reconfigurability of the interface logic in order to be compatible. This is all evidenced by the digital hardware elements Boynton uses.

***Claim Rejections - 35 USC § 102***

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

13. Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by US Pat. 6,973,658 to Nguyen.

14. Per claim 1, Nguyen discloses a universal interface device (*Fig. 1, element 100*), comprising: a controller (*Fig. 1, element 105*); a configuration database coupled to the controller (*Fig. 2, element 210 and Fig. 1, MEMORY element connected to controller; Column 7, lines 50+, discloses storing various drivers, programs, etc, which by definition, is a configuration database*), said configuration database having stored

therein a plurality of different configuration protocols (*Column 7, lines 50+, expressly states memory, element 210, "...is used primarily for storing...initialization program, main program...connector cores, device driver,...", connector cores clearly being protocols for the different connections, see Column 4, lines 48-59*) for supporting a plurality of different peripheral devices (*Fig. 1, elements 184-194 are the various devices working over different protocols*); a plurality of interconnection pads (*Fig. 1, elements 124-129 are the ports/pads/pins associated with each peripheral device*); a memory (*Fig. 2, element 272, internal memory to the programmable unit in Fig. 1; Column 8, lines 5-10 disclose the memory being RAM*) coupled to the interconnection pads and controller, the memory is programmable by the controller in order to support any of the different peripheral devices (*Fig. 2, shows internal memory used to support various protocols*); and a multiplexer coupled between the memory and the plurality of interconnection pads (*Column 13, lines 58-60, the multiplexer is inside the programmable unit, Fig. 1, element 115*) wherein the universal interface device concurrently interfaces with the plurality of different peripheral devices (*Column 4, lines 25-31 discloses two or more peripherals connected at the same time, hence concurrently interfacing two or more devices*) using time multiplexing of the plurality of interconnections pads (*Column 9, lines 3+ disclose "periodically" polling the various I/O ports, elements 125-129 for connection of a external device; Based on the given 35 U.S.C 112 rejection above, the view of time multiplexing using periodic polling suffices the "time multiplexing" limitation since polling is done with respect to time*).

15. Per claim 5, Nguyen discloses claim 1, further disclosing the controller selects the configuration protocol amongst the plurality of protocols (Column 5, lines 43-55) in the configuration database (Column 5, lines 43-55, connector cores stored in configuration database storage, element 120 executed by controller) to configure the memory and support the active peripheral device (Fig. 2, element 272 configured to support active peripheral).

***Claim Rejections - 35 USC § 103***

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

17. Claims 2,4,6,8 and 9 are rejected under 35 USC 103(a) as being unpatentable over Nguyen in view of US Pat. 6,742,071 to Boynton et al. (Boynton).

Nguyen discloses claim 1.

Nguyen does not disclose expressly the use a state machine in the controller and what is required of a state machine that controls a universal interface device. Nguyen also does not disclose a programmable clock coupled to the memory.

Boynton discloses a universal interface device capable of interface various external inputs (Fig. 4; Column 2, lines 30+). Boynton expressly discloses the need for a state machine to handle various situations presented by a universal interface device, where the input signals vary depending on the protocol (Fig. 13 and 14, different read/write and control signals determine how the interface device needs to operate, the

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operation determined by the state machine). Boynton further discloses the state logic (Fig. 13 and 14) interoperating with various parts other digital hardware, as well as the state logic interacting with tri-state devices (Fig. 13 and 14, element 163"). Boynton also discloses the need for a programmable clock signal (Column 2, lines 35-40).

Nguyen and Boynton are analogous art because they are from similar problem solving area in interfacing multiple devices each operating with a different communication protocol, many of the protocols being the same, e.g., USB, and other asynchronous, isochronous, synchronous protocols.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a state machine with the associated logic necessary to communicate with multiple different protocol devices and having a programmable clock signal.

The suggestion/motivation for doing so would have been it being well-known in digital design that state machines operate to oversee and guide how the overall digital logic operate, and in particular, for state machines used in universal interface devices, programmable routing, mapping, programmable clocks, etc. are needed in order to interface with various communication protocols that operate at different frequencies, and require reconfigurability of the interface logic in order to be compatible. This is all evidenced by the digital hardware elements Boynton uses.

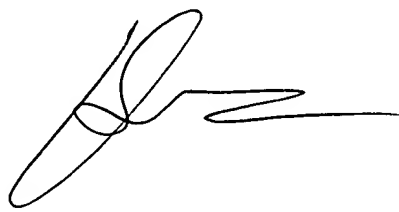
**Conclusion**

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ASC  
11/22/2006



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12/5/06